09/777,576 entitled STRUCTURE AND METHOD FOR A COMPACT TRENCH-CAPACITOR DRAM CELL WITH BODY CONTACT the contents and disclosure of which are incorporated by reference as if fully set forth herein. Described now with reference to Figures 1(a)- 1(f) are the various processing steps for forming vertical DRAM cell arrays. As shown in Figure 1(a), there is depicted an initial structure that is employed in fabricating a vertical DRAM cell array. Specifically, Figure 1(a) shows an array portion of the structure that includes Si-containing substrate 10 having a material stack comprising an etch stop pad layer 12 and a hard mask 14 formed thereon. The substrate may include well regions 11, or the well regions may be formed later in the process.

Amend the paragraph extending between pages 3 and 4 as follows.

An OSS process is then performed which may include the following processing steps: removing a portion of the polysilicon placeholder material using an etch process that is selective to the etch stop liner on a side of the deep trench where a strap is to be formed; removing the exposed collar oxide by utilizing an isotropic oxide etching process; removing portions of the etch stop liner and the node dielectric that are not protected by the remaining region of the polysilicon placeholder material; removing the remaining polysilicon placeholder material; opening a portion of the oxide layer over the deep trench polysilicon not covered by the etch stop liner; continuing the oxide etching so as to form a divot in the top collar oxide at approximately the top level of the deep trench conductor; and filling the divot with a conductive material such as doped polysilicon so as to provide a bridge between the deep trench conductor and the wall of the trench. During a subsequent annealing step, dopant from the divot filled region diffuses forming buried-strap outdiffusion region 24. The

divot filled region is labeled as 26 in the drawings. Note that on the remaining wall portion of the structure not containing buried-strap outdiffusion 24 and divot filled region 26 is an "intact" collar oxide region 18, both directly beneath the divot filled region 26 and also on the wall not having a strap which extends all the way to the etch stop pad layer 12. The intact collar oxide serves to electrically isolate body region 19 from trench capacitor 22.

Please amend the three paragraphs on page 10, lines 4-26, as follows.

After growing the gate oxide 70, the gate conductor polysilicon (or α-Si) deposited as described herein with respect to Figure 1(f). Figure 2(f) illustrates removal of the excess gate poly and the TTO HDP oxide 28 on the top of the pad nitride 14 down to the level of the pad nitride. The gate poly 70 and the TTO HDP 28 on the pad nitride 14 are removed by any of the techniques discussed in commonly-owned, co-pending United States Patent Application Serial No. 09/675,435, entitled AN EXTENDIBLE PROCESS FOR IMPROVED TOP OXIDE LAYER FOR DRAM ARRAY AND THE GATE INTERCONNECTS WHILE PROVIDING SELF-ALIGNED GATE CONTACTS the whole contents and disclosure of which is incorporated by reference as if fully set forth herein.

Figure 2(g) illustrates the next step of removing the pad nitride 14 by stripping it away selective to the gate poly 12 leaving poly pillars 80 extending above the silicon surface, as discussed in co-pending United States Patent Application Serial No. 09/675,435 . An optional Contact to Bitline (CB) etch-stop liner may also be deposited on the substrate surface at this stage in the process. This liner could be selectively removed from the tops of